FIG. 1

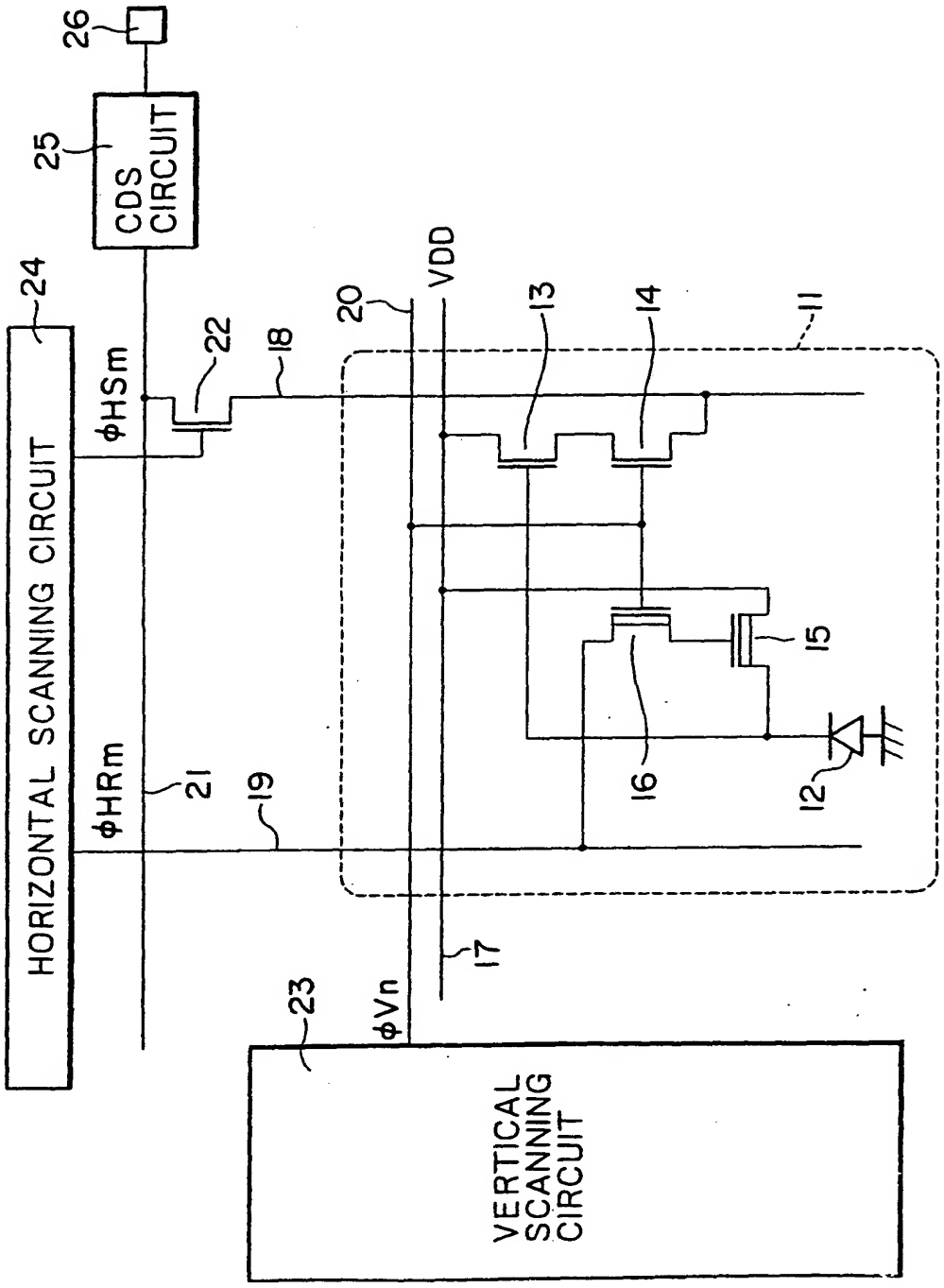

26
25
CDS CIRCUIT
24
HORIZONTAL SCANNING CIRCUIT
φHSm
φHRm
22
18
21
19
20
VDD
13
14
11
15
16
12
17
23
φVn
VERTICAL SCANNING CIRCUIT

FIG. 2

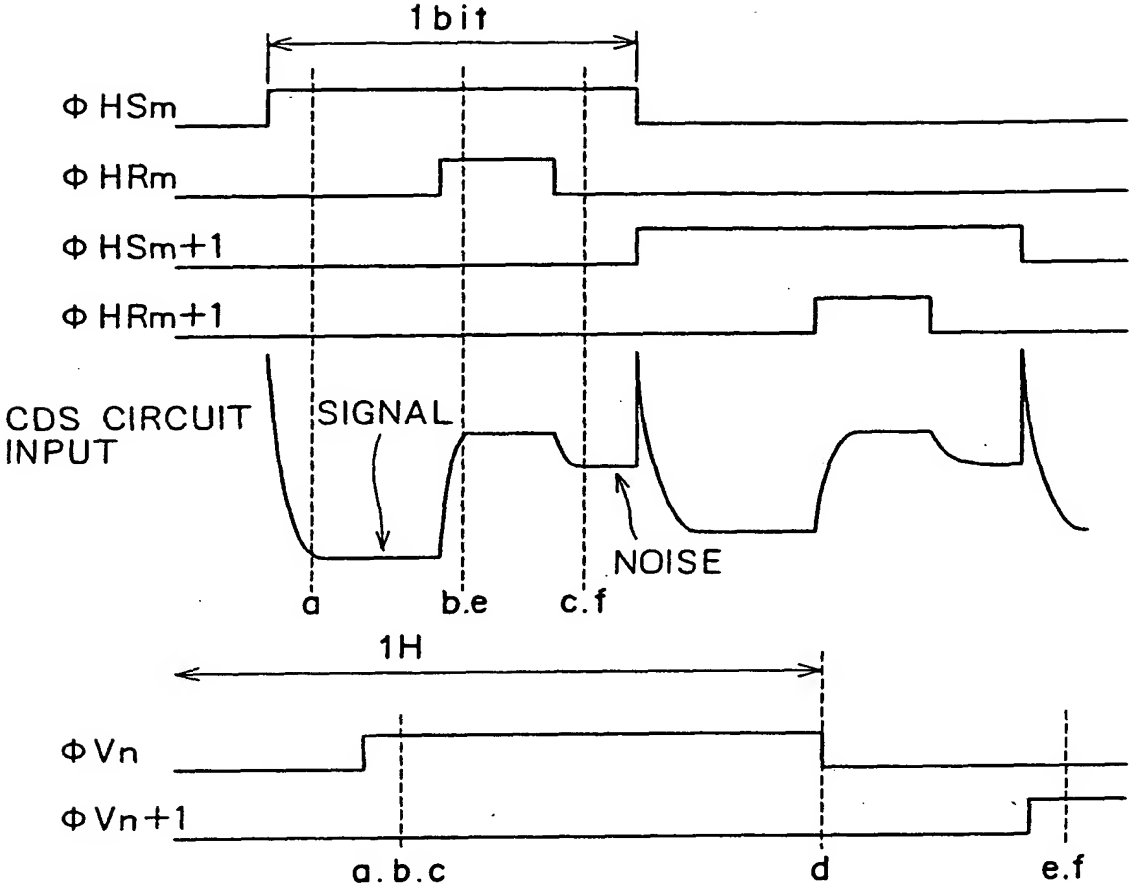

1bit
Φ HSm
Φ HRm
Φ HSm+1
Φ HRm+1
CDS CIRCUIT INPUT
SIGNAL
NOISE
a
b.e
c.f
1H
Φ Vn
Φ Vn+1
a.b.c
d
e.f

FIG. 3

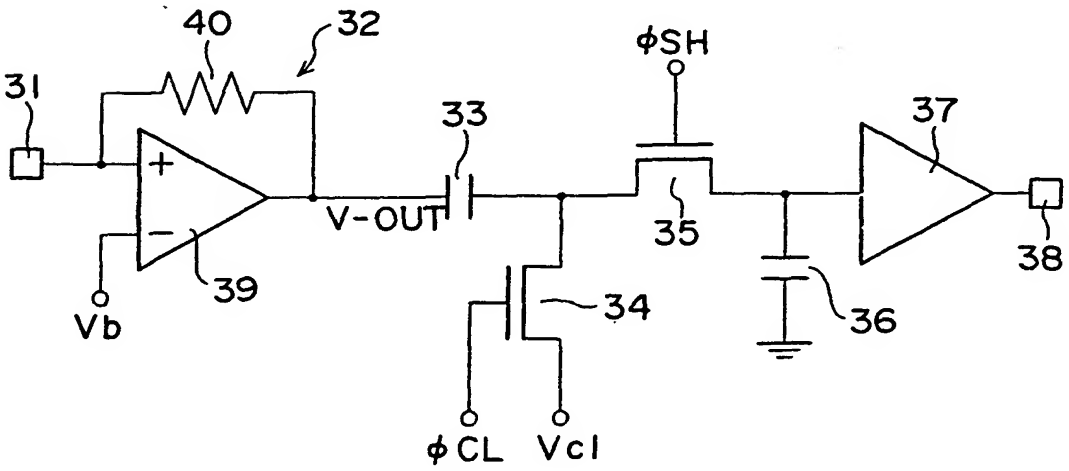

40
32
31
33
φSH
37
V-OUT
35
38
39
Vb
34
36
φCL
Vcl

FIG. 4A

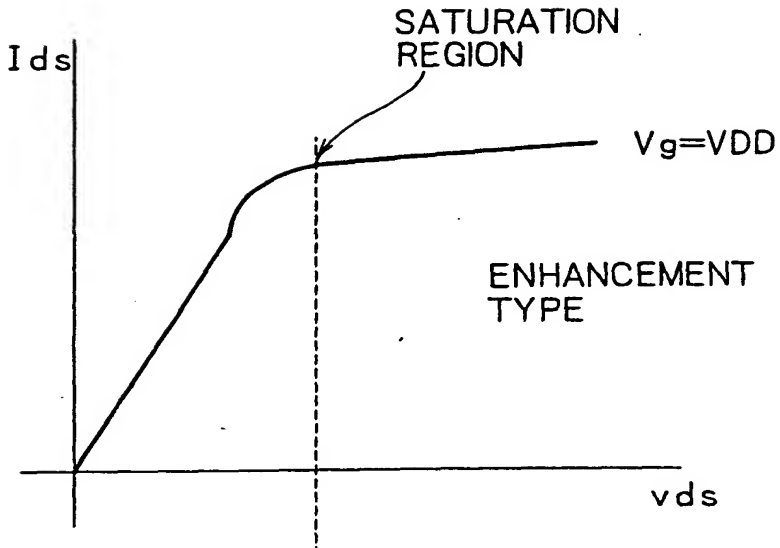

Ids
SATURATION
REGION
Vg=VDD
ENHANCEMENT
TYPE
vds

FIG. 4B

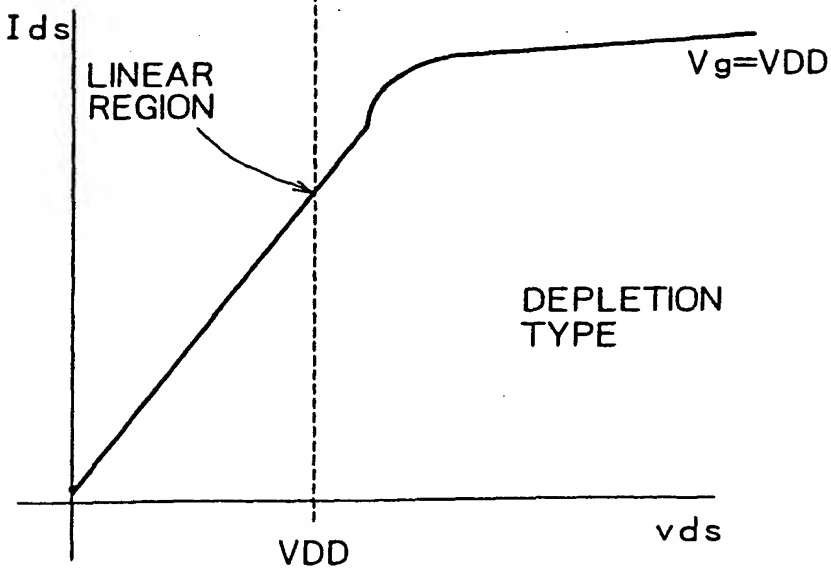
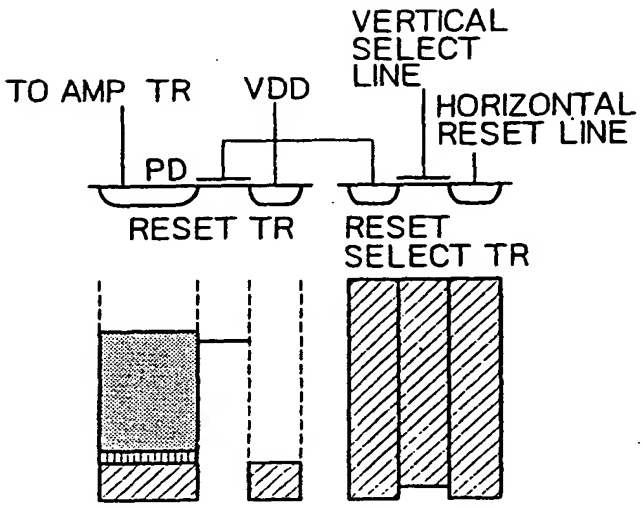
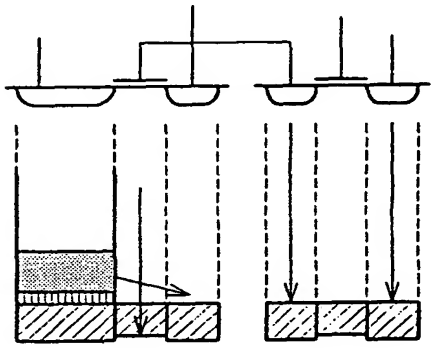

Ids
LINEAR
REGION
Vg=VDD
DEPLETION
TYPE
VDD
vds

FIG. 5

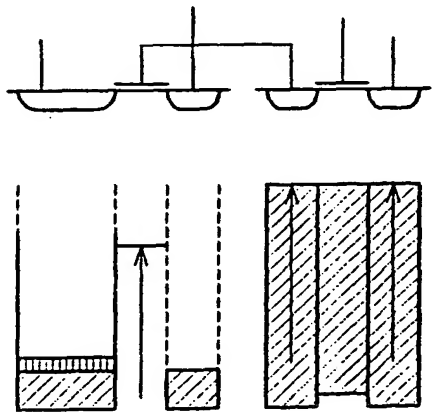
a : SIGNAL READ:
SELECTED PIXEL



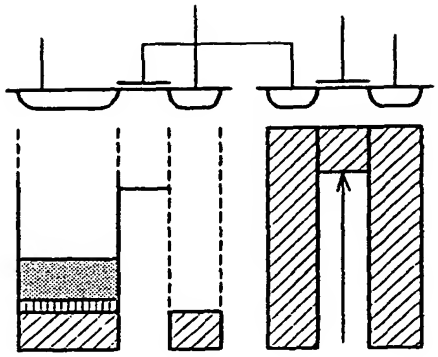
b : PIXEL RESET:
SELECTED PIXEL



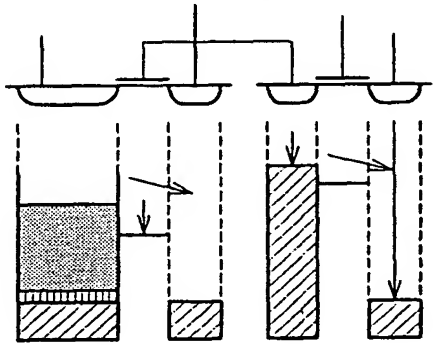
c : NOISE LEVEL READ:
SELECTED PIXEL



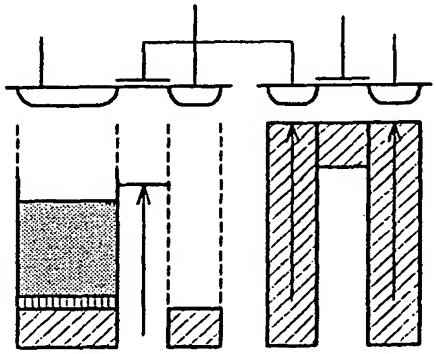
d : STORAGE



e : PIXEL RESET:
NONSELECTED PIXEL



f : NOISE LEVEL READ:
NONSELECTED PIXEL



DRAIN LEVEL

SIGNAL CHARGE

RESET GATE
FEEDTHROUGH

FIG. 6

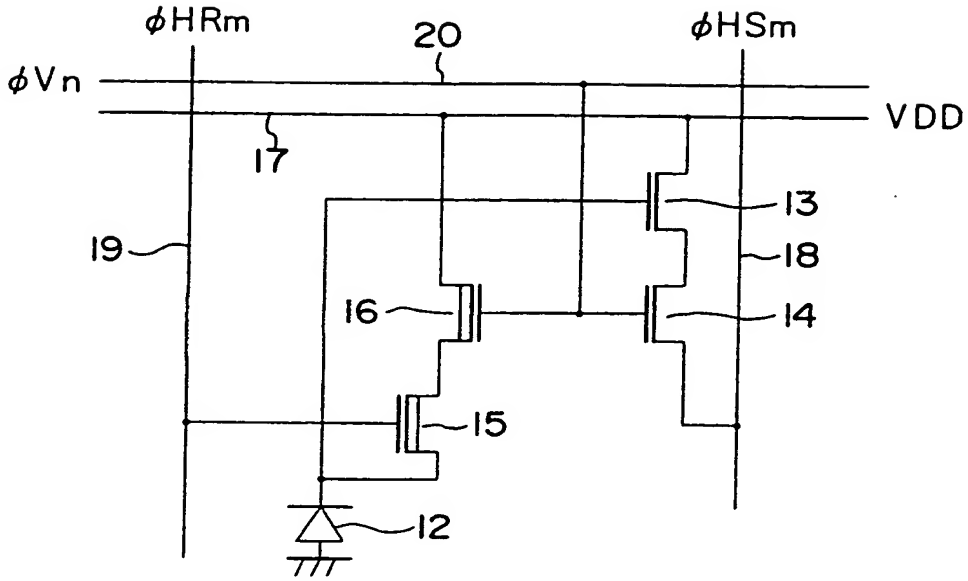

φHRm
20
φHSm
φVn
VDD
17
13
19
18
16
14
15
12

FIG. 7

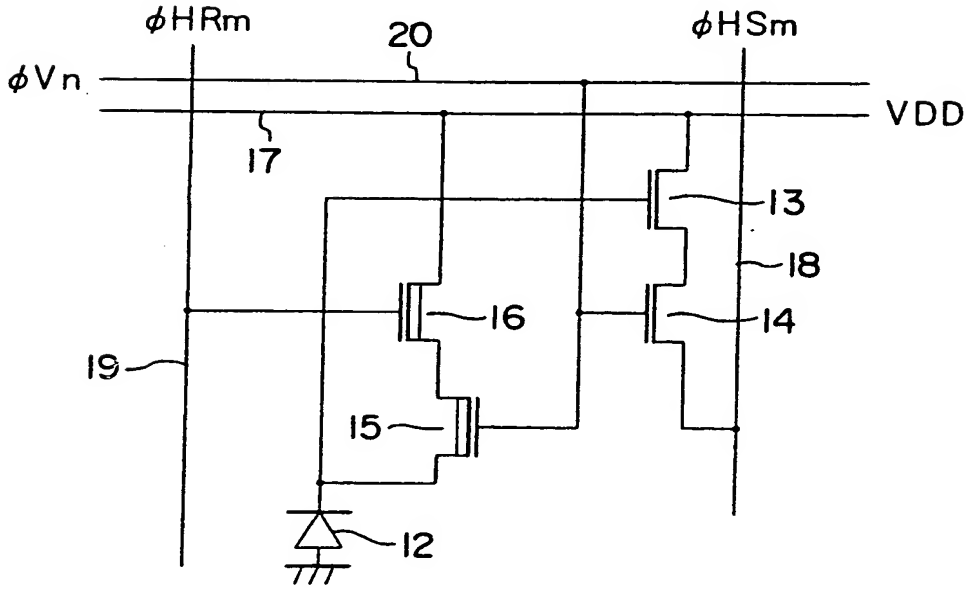

φHRm
20
φHSm
φVn
VDD
17
13
18
16
14
19
15
12

FIG. 8

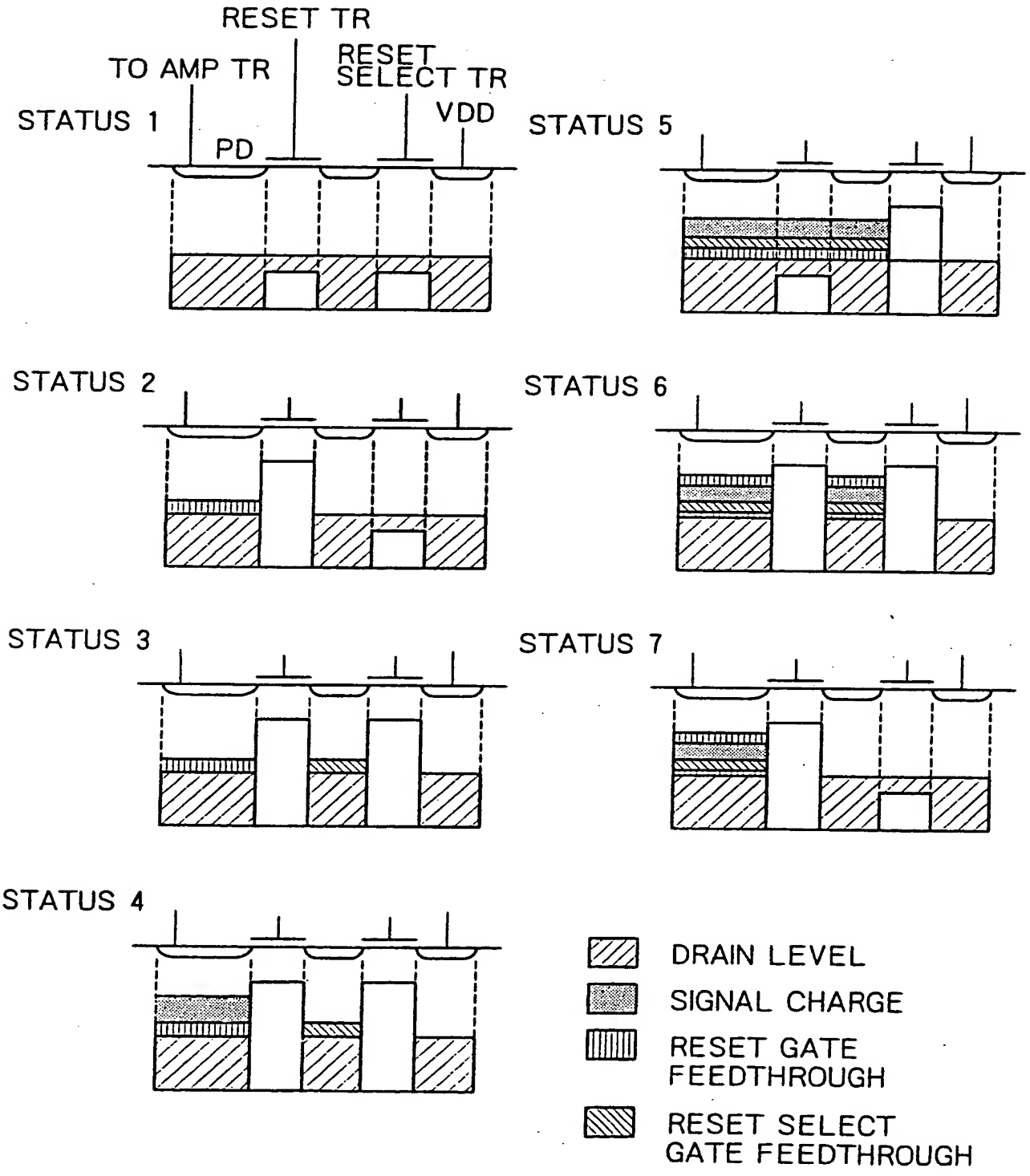

RESET TR
TO AMP TR
RESET SELECT TR
VDD
PD
STATUS 1
STATUS 2
STATUS 3
STATUS 4
STATUS 5
STATUS 6
STATUS 7
DRAIN LEVEL
SIGNAL CHARGE
RESET GATE FEEDTHROUGH
RESET SELECT GATE FEEDTHROUGH

FIG. 9

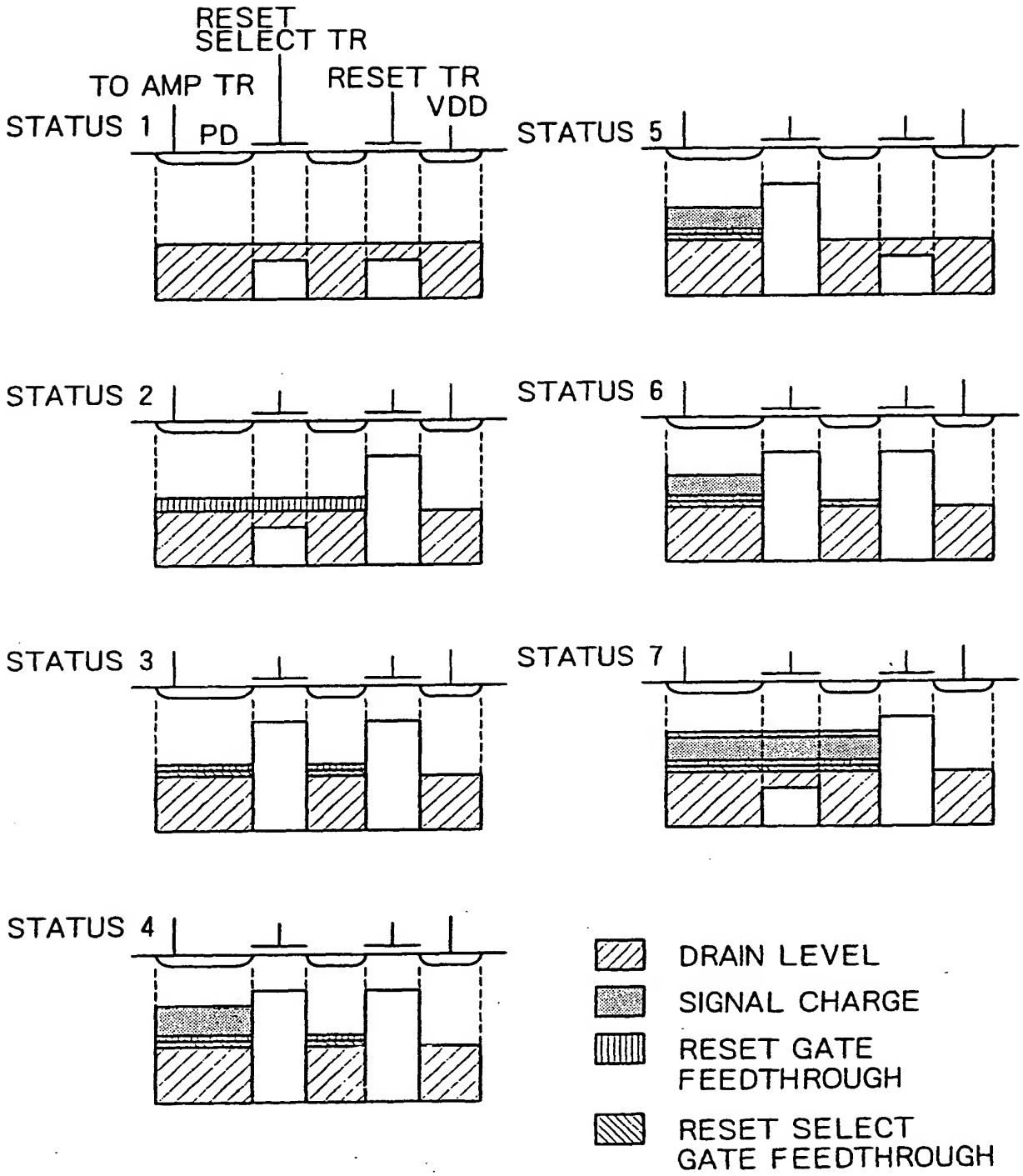

RESET
SELECT TR
TO AMP TR
RESET TR
VDD
STATUS 1
PD
STATUS 5
STATUS 2
STATUS 6
STATUS 3
STATUS 7
STATUS 4
DRAIN LEVEL
SIGNAL CHARGE
RESET GATE
FEEDTHROUGH
RESET SELECT
GATE FEEDTHROUGH

FIG. 10

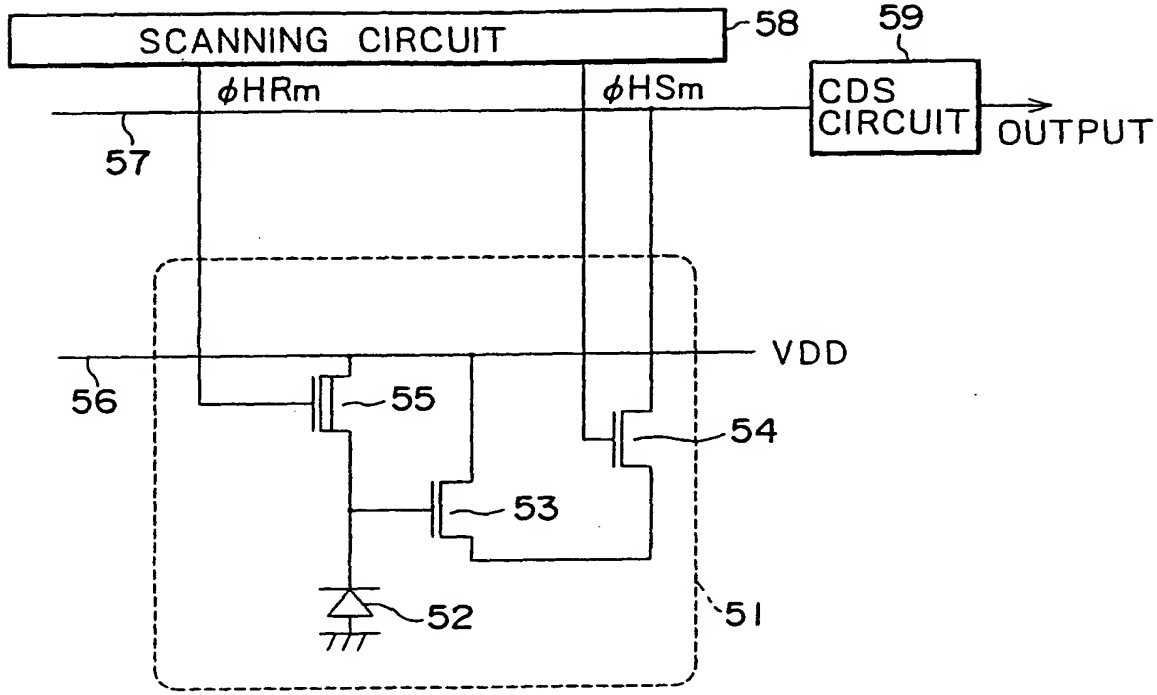

SCANNING CIRCUIT
58
59
φHRm
φHSm
CDS CIRCUIT
OUTPUT
57
VDD
56
55
54
53
52
51

FIG. 11

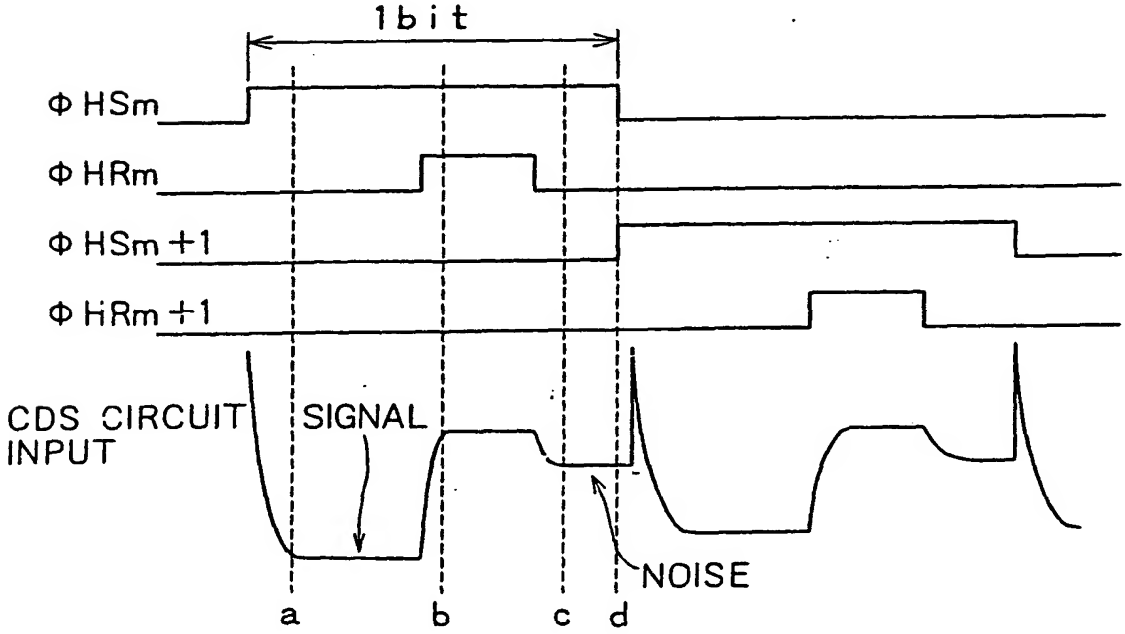

1bit
Φ HSm
Φ HRm
Φ HSm+1
Φ HRm+1
CDS CIRCUIT INPUT
SIGNAL
NOISE
a
b
c
d

FIG. 12

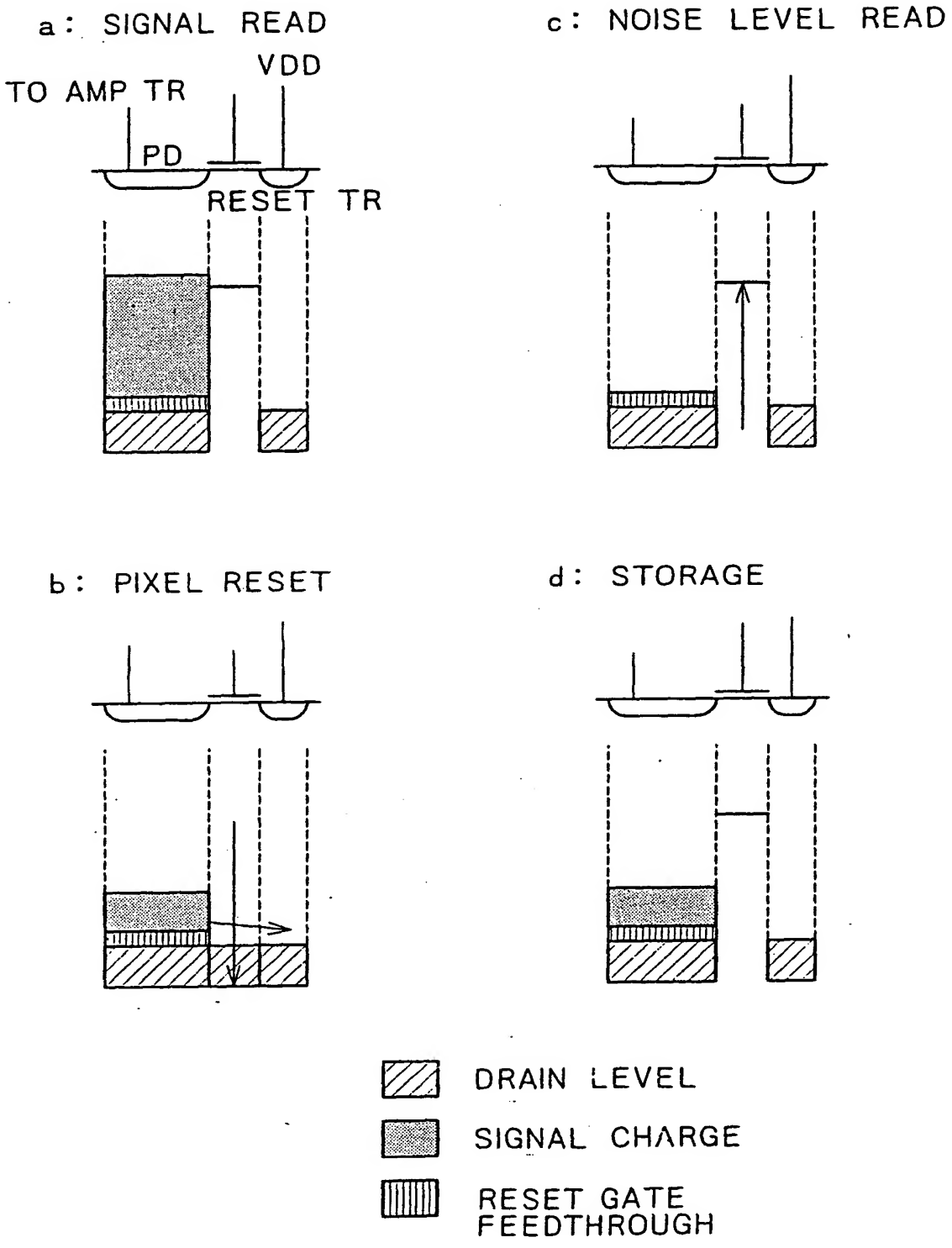

a : SIGNAL READ
VDD
TO AMP TR
PD
RESET TR
c : NOISE LEVEL READ
b : PIXEL RESET
d : STORAGE
DRAIN LEVEL
SIGNAL CHARGE
RESET GATE FEEDTHROUGH

FIG. 13

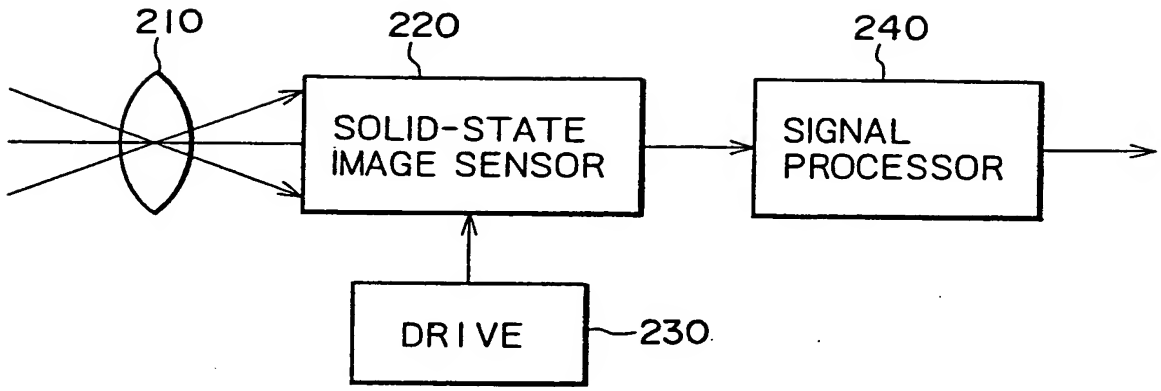


FIG. 14 (RELATED ART)

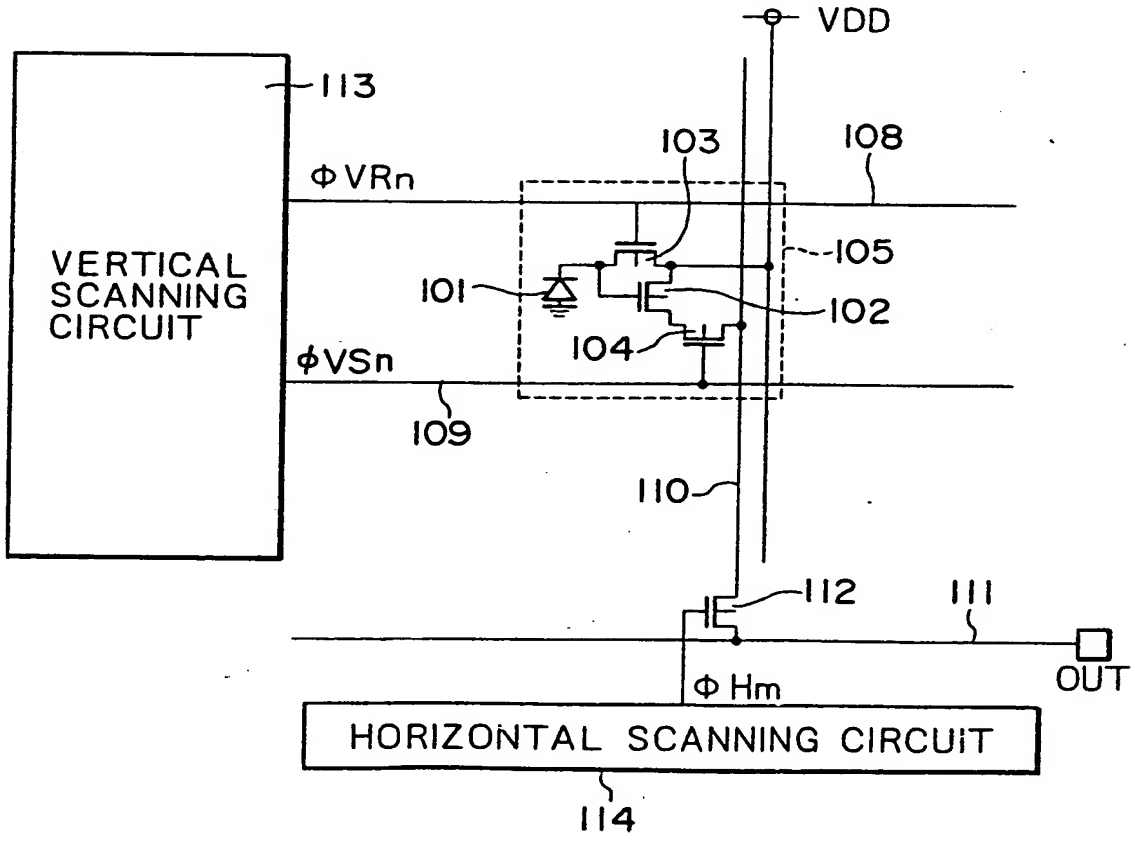
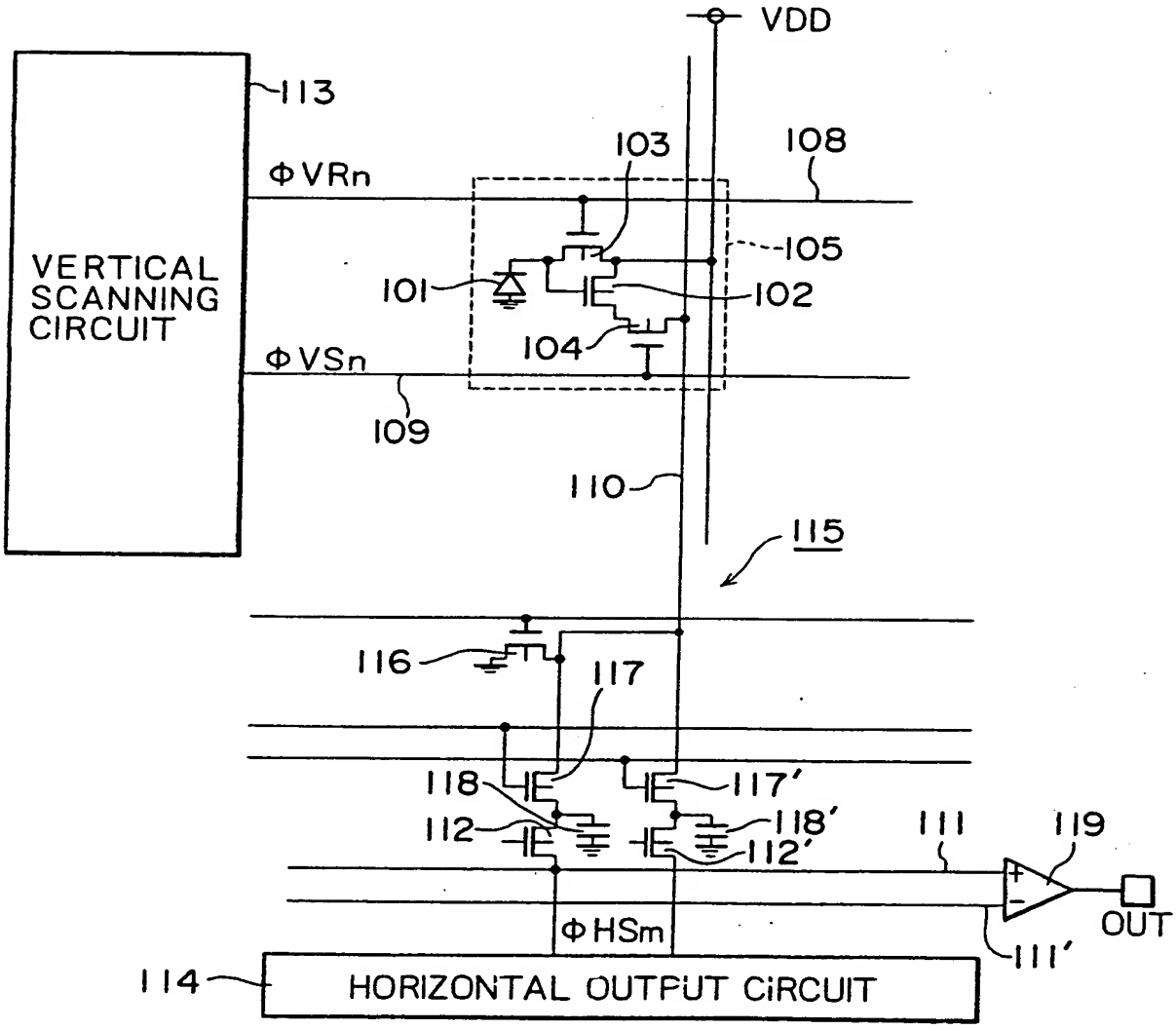


FIG. 15


VDD
113
VERTICAL SCANNING CIRCUIT
ΦVRn
103
108
105
101
102
104
ΦVSn
109
110
115
116
117
118
117'
112
118'
112'
111
119
OUT
ΦHSm
111'
114
HORIZONTAL OUTPUT CIRCUIT